REMARKS

I. Introduction

In response to the Office Action mailed January 24, 2005, Applicants have rewritten claim 1 so as to further clarify the claim language as kindly suggested by the Examiner. Also, the Title of the Invention has not been amended in the manner as suggested by the Examiner, so that the title as amended in the previous amendment can *generically* describe all the embodiments of the present invention. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1-3, 5, 7-10, 12-15 and 21 stand rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 5,506,976 to Jaggar. Applicants respectfully traverse this rejection for at least the following reasons.

In the October 12, 2004 response, Applicants argued, "Jaggar discloses that the comparator 14 compares the lowermost eight bits between the program counter value PC and the reach value R ..., which is a preliminary comparison before the program counter value PC is compared with the cache tags within the branch cache 4." In response, the Examiner merely asserted, "Applicant appears to be arguing limitations which are not in the claim, and it is not clear how performing a preliminary comparison differs from comparing address one by one."

As a preliminary matter, it is not entirely understood which limitations the Examiner alleges as not appearing in the claims. In fact, it appears the Examiner has misunderstood Applicants' previous arguments. Specifically, in the previous response, Applicants were NOT arguing that the

present invention ***requires*** a preliminary comparison. Instead, Applicants were arguing that the present invention does ***not*** require a preliminary comparison as demonstrated by Jaggar, in which the comparator 14 ***specifically*** compares the reach value R currently stored in the reach value latch 16 with the lower order bits (i.e., lowermost eight bits) of the program counter value PC in the 16-bit addresses stored in the program counter register 10. In this regard, the comparator 14, at best, merely compares the contents of the reach value latch 16 with the program counter value PC so as to determine whether to hold the enable signal in the OFF state. That is, the alleged detection or comparison performed by the comparator 14 of Jaggar is merely a preliminary comparison and is actually ***irrelevant*** to the actual determination of the last instruction. In other words, Jaggar is completely silent as to utilizing a comparator that can determine whether the comparison performed therein is the last instruction. Accordingly, Applicants' argument that Jaggar expressly discloses a preliminary comparison was ***not*** intended to imply that Applicants' claims require a preliminary comparison such that "Applicant appears to be arguing limitations which are not in the claim" as asserted in the pending rejection, but instead, the argument was intended to evidence that Jaggar does not disclose detecting the last instruction using the comparator 14 in the manner perceived by the Examiner.

Furthermore, Applicants stated that "the detecting means compares the addresses, such as fetch address and end address, one by one" and that "the detecting means of the present invention is fundamentally different from the alleged detecting means of Jaggar." In response, the Examiner asserted, "it can be seen that each and every address is compared to a reach value" and "...so address &E corresponds to the last instruction before a branch if a cache hit occurs."

However, it is respectfully submitted that this statement as a prelude to the rejection is not a proper basis for rejecting Applicants' claims, as the statement is directed to the ***Examiner's opinion***

rather than what is taught by the prior art. It is submitted that the "Examiner's opinion" cannot be relied on to replace the deficiency of a prior art reference. If the pending rejection intended to take Official Notice that the differences between Jaggar and the present invention as recited in the rejected claims are well-known in the art, then pursuant to **M.P.E.P. § 2144.03**, Applicants respectfully traverse such an assertion and request the Examiner to cite one or more references in support of this position (see, second paragraph, last three lines of **M.P.E.P. § 2144.03**, which requires the Examiner to cite a reference in support of his allegation of Official Notice when Applicants traverse).

Even assuming *arguendo* that the Examiner's opinion has merit, this ***incomplete*** analysis overlooks and ignores the fact that Jaggar expressly discloses that if the lowermost eight bits of the program counter value PC match the value in the reach value latch 16, the enable signal is asserted ON and the value of the full instruction address from the program counter register 10 is compared with the cache tags (see, col. 8, lines 21-25). That is, if the program counter value PC is found to match with the reach value R, ***another*** comparison is performed so as to determine whether a branch cache hit has occurred. Indeed, it is respectfully submitted that only ***after*** the comparator 14 has performed the necessary comparison between the reach value R in the reach value latch 16 and the lowermost eight bits of the program counter value PC stored in the program counter register 10 will there be an ON enable signal asserted (see, col. 6, line 63 to col. 7, line 5), at which point the value of the full instruction address from the program counter register 10 is compared. Accordingly, as discussed above, the alleged detection for detecting a last instruction (i.e., the comparison performed by the comparator 14 of Jaggar) is ***irrelevant*** to the actual determination of the last instruction, and it is respectfully submitted that the Examiner's position departs from what is disclosed in Jaggar; namely, ***the actual detection of the last instruction is performed in the branch***

cache 4 so as to determine a genuine cache hit, and is not performed in the comparator 14 as noted by the fact that branching is not performed even if the lowermost eight bits of the program counter value PC match the value in the reach value latch 16. In this regard, it is important to recognize that if the enable signal of Jaggar is in the ON state, the value of the full instruction address from the program counter register 10 is compared ***in parallel*** with ***all*** of the cache tags so that Jaggar is silent with regard to comparing the full instruction address and each of the cache tags ***one by one***.

In contrast, the detecting means of the present invention detects by comparing information on the instruction to be executed with predetermined information on the process one by one. For example, as illustrated in the example shown at page 18, line 24 to page 20, line 26 of the specification, when the relative address stored in the program counter 134 becomes (0010), the absolute address output from the adder 135 becomes (0110). At this state, because the absolute address matches the end address stored in the end address storing part 121, an end address match signal is output from the comparator 136 (e.g., comparing information on the instruction to be executed with predetermined information on the process in processing) to the read-out selection controller 133, the program counter 134, and the supervisory processor 151. Then, the selectors 131 and 132 are respectively switched to select the start address storing part 112 and the end address storing part 122 so that the comparator 136 can compare the end addresses stored in the end address storing parts 122 with the fetch address.

Moreover, Applicants previously argued, "Jaggar requires that the branch instruction detector 22 detects the last instruction before branching by detecting the branch instruction in order to automatically set the cache data in each cache line 12" and "the present invention does not require such a branch instruction detector for detecting the last instruction before branching any

instruction." In response, the Examiner asserted, "Applicant is arguing limitations that are not in the claim" and "it is not clear how the system may initially detect the last instruction before the branch without knowing where the branch is located."

However, similar to the reasons as set forth above, it is not entirely understood which limitations the Examiner alleges as not appearing in the claims. Once again, it appears the Examiner has misinterpreted Applicants' previous arguments. Specifically, in the previous response, Applicants were NOT arguing that the present invention ***requires*** a branch instruction detector. Instead, Applicants were arguing that the present invention does ***not*** require such a branch instruction detector for detecting the last instruction as demonstrated by Jaggar, and that the Applicants' argument was intended to evidence that Jaggar does not disclose a detecting means that can be reasonably interpreted as the claimed detecting means.

Also, the Examiner's further question of how the system may initially detect the last instruction before the branch without knowing where the branch is located is a matter of ***scope*** and not of ***clarity***. It is respectfully submitted that the pending claims do ***not*** have to disclose how the last instruction is initially detected as alleged by the Examiner. Additionally, it is important to note that the pipeline processor 2 of Jaggar is a branch cache device as known in the art in which an address of the last instruction of each process is stored in the cache line 12 of the branch cache 4, such that all the addresses stored therein are compared in parallel with the program counter value PC despite of any process in progress. In this manner, the address of the last instruction must be stored in the cache line 12 every time a branch instruction is detected, which is realized by the branch instruction detector 22.

In direct contrast, in accordance with one exemplary embodiment of the present invention, the last instruction of a process before branching is detected in the manner as described, for

example, at page 15, line 27 to page 16, line 8 of the specification. More specifically, when the current execution instruction address does not match with the end address, the program counter 134 is counted up and the processes after the step ST12 are repeated. On the other hand, when the current execution instruction address matches with the end address, the comparator 136 outputs an end address match signal to the read-out selection controller 133, the program counter 134 and the supervisory processor 151. Specifically, an end address match signal is input to the read-out selection controller 133, and the read-out selection controller 133 outputs a read-out selection signal for selecting one of the address storing parts 111 to 113 storing the start address and one of the address storing parts 121 to 123 storing the end address of the next program module to be processed to the selectors 131 and 132, respectively. As such, because the last instruction can readily be determined via, for example, the program counter 134, comparator 136, read-out selection controller 133 and the selectors 131/132, the present invention does not require any branch instruction detector as required in the cited prior art. For all of the foregoing reasons, it is respectfully submitted that Jaggar does not disclose a detecting means that can be reasonably interpreted as the claimed detecting means.

Also, with respect to claim 5, this claim recites in-part wherein the detecting means detects the last instruction based on judgment whether information stored ... in the storing means indicates the last instruction. In the pending rejection, the Examiner asserts, "... each instruction address is compared to the predetermined reach value ...." However, in formulating this argument, it is clear that the Examiner departs from what is disclosed in Jaggar; namely, the alleged information or "each" instruction address is clearly ***not*** stored in the main memory system 8 or the alleged storing means as required by claim 5. Also, the alleged information is merely an instruction address, rather

than an information that indicates a last instruction. For these reasons, it is respectfully submitted that claim 5 is patentable over the cited prior art.

As a final note, it is noted that the Examiner asserted that "... [the advantages of the present invention and the disadvantages of Jaggar] have nothing to do with the fact that Jaggar anticipates the current language of the claims (see, page 18, 2nd paragraph of Office Action)." However, the Examiner appears to ignore these advantages of the present invention and the disadvantages of Jaggar without knowing that these arguments are stemmed from the fact that " ... the program counter value PC [of Jaggar] must be compared ***in parallel*** with the cache tag values of each of the cache lines 12..." and "the comparator 14 of Jaggar compares ***two values*** preliminarily ...," while "the detecting means [of the present invention] compares, e.g., the addresses, such as fetch address and end address, ***one by one***" and "the detecting means of the present invention detects ... a ***last instruction*** of a process before branching." In other words, Jaggar does not anticipate the claimed structural elements recited by the pending claims, because the alleged features disclosed in Jagger do not operate in the manner recited by claimed elements, and is ***further evidenced*** by the fact that Jagger does not disclose or suggest any of the associated structural benefits, identified only by Applicants.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Jaggar fails to disclose the foregoing claim elements, it is clear that Jaggar does not anticipate claim 1 or 5, or any of the claims dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as claims 1 and 5 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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